IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claim 15 without prejudice or disclaimer of the subject matter therein, ADD claim 16 and AMEND claims 11 and 12 in accordance with the following:

1. (Original) A method of fabricating a TFT using dual or multiple gates comprising:

calculating a probability including Nmax (the maximum number of crystal grain boundaries in active channel regions according to the length of the active channels); and

adjusting a gap between the active channels capable of synchronizing the number of the crystal grain boundaries in each active channel region of the TFT using the dual or multiple gates in the case where Gs, the size of crystal grains of polycrystalline silicon forming a TFT substrate, θ angle in which the "primary" crystal grain boundaries are inclined at a direction perpendicular to an active channel direction of the gates, the width of the active channels and the length of the active channels are determined.

2. (Original) The method of claim 1, wherein the probability is calculated as follows:

$$P=(D-(Nmax-1)XGs)/Gs$$

where $D=L\cos\theta+W\sin\theta$, L is the length of active channels of the TFT, W is the width of the active channels of the TFT, Nmax is the maximum number of "primary" crystal grain boundaries that can be contained in the active channel regions of a TFT having the length L and the width W, Gs is the size of crystal grains, θ is an angle in which the "primary" crystal grain boundaries are inclined at a direction perpendicular to an active channel direction of the TFT, m is an integral number greater than 0, and W is the width of each active channel of the TFT having the dual or multiple gates.

3. (Original) The method of claim 1, wherein the gap between the active channels is calculated as follows:

$S=mGs \cdot \sec\theta-L$

where Gs is the size of crystal grains, θ is an angle in which fatal crystal grain boundaries ("primary" crystal grain boundaries) are inclined at a direction perpendicular to an active channel direction, and L is the length of each active of each of dual or multiple gates.

4. (Original) The method of claim 3, wherein the angle is $-45° \leq \theta \leq 45°$.

5. (Original) The method of claim 3, wherein the gap between the active channels is adjusted so that the probability is not 0.5.

6. (Original) The method of claim 2, wherein the gap between the active channels is calculated as follows:

$S=mGs \cdot \sec\theta-L$

where Gs is the size of crystal grains, θ is an angle in which fatal crystal grain boundaries ("primary" crystal grain boundaries) are inclined at a direction perpendicular to an active channel direction, and L is the length of each active channel of each of dual or multiple gates.

7. (Original) The method of claim 6, wherein the angle is $-45° \leq \theta \leq 45°$.

8. (Original) A method of fabricating a TFT using dual or multiple gates comprising:

calculating a first probability in which Nmax, the maximum number of "primary" crystal grain boundaries capable of judging uniformity in TFT characterstics during fabrication of a TFT substrate using large silicon grains are included in active channel regions on the total substrate of a display device; and

using dual or multiple gates using the first probability to judge optimum process conditions on size and direction of silicon crystal grains and optimum dimensions of the active channels to secure uniformity of the TFT characteristics.

9. (Original) The method of claim 8, wherein the probability is calculated as follows:

$P=(D-(N_{max}-1)XGs)/Gs$

where $D=L\cos\theta+W\sin\theta$, L is the length of active channels of the TFT, W is the width of the active channels of the TFT, Nmax is the maximum number of "primary" crystal grain boundaries that can be contained in the active channel regions of a TFT having the length L and the width W, Gs is the size of crystal grains, θ is an angle in which the "primary" crystal grain boundaries are inclined at a direction perpendicular to an active channel direction of the TFT, m is an integral number greater than 0, and L is the length of each active channel of the TFT having the dual or multiple gates.

10. (Original) The method of claim 8, wherein the gap between the active channels is calculated as follows:

$$S=mGs \cdot \sec\theta-L$$

where Gs is the size of crystal grains, θ is an angle in which fatal crystal grain boundaries ("primary" crystal grain boundaries) are inclined at a direction perpendicular to an active channel direction, and L is the length of each active of each of dual or multiple gates.

11. (Currently Amended) The method of claim ~~3~~10, wherein the angle is $-45^\circ \le \theta \le 45^\circ$.

12. (Currently Amended) The method of claim ~~3~~10, wherein the gap between the active channels is adjusted so that the probability is not 0.5.

13. (Original) The method of claim 9, wherein the gap between the active channels is calculated as follows:

$$S=mGs \cdot \sec\theta-L$$

where Gs is the size of crystal grains, θ is an angle in which fatal crystal grain boundaries ("primary" crystal grain boundaries) are inclined at a direction perpendicular to an active channel direction, and L is the length of each active channel of each of dual or multiple gates.

14. (Original) The method of claim 13, wherein the angle is $-45^\circ \le \theta \le 45^\circ$.

15. (Cancelled)

16. (New) A method of fabricating a TFT using dual or multiple gates comprising:

calculating a maximum number of crystal grain boundaries in each of active channel regions of the TFT according to a length and width of the active channel regions;

determining a major axis direction size of crystal grains;

determining an angle of inclination of the crystal grain boundaries with respect to the active channel direction of the gates; and

adjusting a gap between the active channel regions to determine the maximum number of crystal grain boundaries in each of the active channel regions based on the calculated maximum number of crystal grain boundaries, the determined major axis, the determined angle of inclination and the determined width and length of the active channel regions.